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loop and queue and registers

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Tyson, G.S.; Smelyanskiy, M.; Davidson, E.S.;

Computers, IEEE Transactions on , Volume: 50 , Issue: 8 , Aug. 2001

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Smelyanskiy, M.; Tyson, G.S.; Davidson, E.S.;

Parallel Architectures and Compilation Techniques, 2000. Proceedings.

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Pages:3 - 12

[\[Abstract\]](#) [\[PDF Full-Text \(940 KB\)\]](#) **IEEE CNF****3 Evaluating the use of register queues in software pipelined loops**

Tyson, G.S.; Smelyanskiy, M.; Davidson, E.S.;

Computers, IEEE Transactions on , Volume: 50 , Issue: 8 , Aug. 2001

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[\[Abstract\]](#) [\[PDF Full-Text \(3240 KB\)\]](#) **IEEE JNL****4 Partitioned schedules for clustered VLIW architectures**

Fernandes, M.M.; Llosa, J.; Topham, N.;

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